

Xenotran's 181C Modules

FPGA Hardware

TIMERS

MODULATOR CHIP/FRAME TIMER
DEMULATOR CHIP/FRAME TIMER
SATELLITE CHIP/FRAME TIMER

MODULATOR

DIGITAL INTERMEDIATE FREQUENCY (IF) LOCAL OSCILLATOR
DIGITAL SYNTHESIS CPM SYMBOL PHASE MODULATION
DIGITAL SYMBOL TIMING
TRANSMITTER CONTROL

DEMULATOR

DIGITAL IF LOCAL OSCILLATOR
DIGITAL MIXER
DIGITAL DOWN-CONVERTER
MATCHED FILTER BANK
COHERENCE LOCK
CONTINUOUS PHASE MODULATION (CPM) DEMODULATOR
MINIMUM SHIFT KEYING (MSK) DEMODULATOR
EARLY DECISION GENERATOR
SOM DETECTOR
PHASE LOCKED LOOP (PLL)
SYMBOL TIMING LOOP (STL)
FAST FOURIER TRANSFORM (FFT)
DEMULATOR STATE MACHINE

MODELING AND TEST

ADDITIVE WHITE GAUSSIAN NOISE (AWGN) MODEL
C/KT ATTENUATOR
DOPPLER SWEEP GENERATOR
TEST-POINT MULTIPLEXOR

DSP Software

MODULATOR

BURST TRANSMISSION REQUEST

QUEUING

PARSING

SCHEDULING

PREAMBLE GENERATION
MSK MODULATOR
CPM MODULATOR
CPM PADDING AND POSTAMBLE GENERATION
CPM TERMINATOR
MESSAGE TRANSMISSION CONTROL AND TIMING

DEMODULATOR

CPM DEMODULATOR
MSK DEMODULATOR
SOM DETECTOR
ACQUISITION ANALYSIS
SPECTRUM THRESHOLDER
PHASE ESTIMATOR
DOPPLER FREQUENCY ESTIMATOR
SYMBOL TIMING ESTIMATOR
RANGE REPORTING
POSTAMBLE DETECTION
RECEIVER STATE MACHINE
MESSAGE ACQUISITION TIMING AND TRACKING
BURST RECEPTION REQUEST
QUEUING
PARSING
SCHEDULING
COLLECTION
RELAY

MODELING AND TEST

PROFILE TRACKING
LOGGING
EXPERIMENTAL OPTIONS
(SPECTRAL ANALYSIS, CUSTOM PREAMBLES, ETC.)

Host Software

USER INTERFACE (GUI AND ASCII CONSOLE)
TRANSMISSION/RECEPTION ACTIVATION
TEST DATA GENERATION
BERT TESTING AND REPORTING