

Design Margin

- Design Margin: Difference between Theory (Upper Bound) and Specification (MIL-STD-188-181C)
- Lower numbers are worse (reddish)
- A monolithic design must accommodate as a Design Requirement the worst case of any single mode for the design of common elements (filters, PLL, STL, Preamble initialization errors, etc.)
- 28K CPM modes are surprisingly generous

Design Requirement

Option	Mod	Rate	1E-3	1E-5
13	cpm	2400	1.5352	1.6082
16	cpm	3000	1.3653	1.2946
18	cpm	3600	1.9077	1.289
20	cpm	4000	1.6923	1.5681
21	cpm	4800	2.6005	2.7763
22	cpm	2400	1.5352	1.6082
23	cpm	3000	1.3653	1.2946
24	cpm	3600	1.9077	1.289
25	cpm	4000	1.6923	1.5681
26	cpm	4800	2.6005	2.7763
131	cpm	4800	1.5249	1.0979
136	cpm	4800	1.5249	1.0979
137	cpm	9600	1.5146	1.5876
139	cpm	14400	1.3871	1.2684
141	cpm	16000	1.9296	1.8108
143	cpm	19200	1.8799	1.2557
144	cpm	24000	1.9108	1.7866
145	cpm	28000	3.9474	4.6706
146	cpm	9600	1.5146	1.5876
147	cpm	14400	1.3871	1.7684
148	cpm	16000	1.9296	1.8108
149	cpm	19200	1.8799	1.7557
150	cpm	24000	1.9108	2.2866
151	cpm	28000	3.9474	4.6706
152	cpm	4800	1.5249	1.0979
153	cpm	4800	1.5249	1.0979